GPI WEB CLIENT

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Search Results - *92 Hits.*

Term	Occurrence
L2 (0P) (COMMUNICAT###/BI OR INTERFAC###/BI OR TRANSFER####/BI)	92
COMMUNICAT###/BI	180283
INTERFAC###/BI	59590
TRANSFER####/BI	270271

Database: US Patents / Japanese Patents / European Patents / USOCR Patents

Refine Search:

l2 (p) (communicat### or interfac### or transfer####)

Search History

DB Name	Query	Hit Count	Set Name	Time
JPO	l2 (p) (communicat### or interfac### or transfer####)	92	L4	Tue Feb 23 16:19:26 1999
JPO	l2 and (communicat### or interfac### or transfer####)	104	L3	Tue Feb 23 16:18:20 1999
JPO	process### (p) (programmable) (p) (bus### or line#)	231	L2	Tue Feb 23 16:15:06 1999
JPO	process### (p) (programmable(w) cell#) (p) (bus### or line#)	0	L1	Tue Feb 23 16:12:44 1999

Z39.50 Gateway Based on **CNIDR** Isite

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Search Results - *198 Hits.*

Term	Occurrence
L2 (0P) (COMMUNICAT###/BI OR INTERFAC###/BI OR TRANSFER####/BI)	198
PROCESS###/BI	423537
PROGRAMMABLE/BI	11565
BUS###/BI	22151
LINE#/BI	175790
COMMUNICAT###/BI	79739
INTERFAC###/BI	28702
TRANSFER####/BI	93819

Database: US Patents / Japanese Patents / European Patents / USOCR Patents

Refine Search:

l2 (p) (communicat### or interfac### or transfer####)

Search History

DB Name	Query	Hit Count	Set Name	Time
EPO	l2 (p) (communicat### or interfac### or transfer####)	198	L5	Tue Feb 23 16:20:35 1999
JPO	l2 (p) (communicat### or interfac### or transfer####)	92	L4	Tue Feb 23 16:19:26 1999
JPO	l2 and (communicat### or interfac### or transfer####)	104	L3	Tue Feb 23 16:18:20 1999
JPO	process### (p) (programmable) (p) (bus### or line#)	231	L2	Tue Feb 23 16:15:06 1999
JPO	process### (p) (programmable(w) cell#) (p) (bus### or line#)	0	L1	Tue Feb 23 16:12:44 1999

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Search Results - *0 Hits.*

Term	Occurrence
L4 AND (DATA/BI (0W) FLOW/BI (0W) PROCESSOR#/BI)	0
DATA/BI	472225
FLOW/BI	231597
PROCESSOR#/BI	101044
DATA/BI (0W) FLOW/BI (0W) PROCESSOR#/BI	60

Database: US Patents / Japanese Patents / European Patents / USOCR Patents

Refine Search:

```
l4  and (data(w) flow(w) processor#)
```

Search History

DB Name	Query	Hit Count	Set Name	Time
JPO	l4 and (data(w) flow(w) processor#)	0	L6	Tue Feb 23 16:24:47 1999
EPO	l2 (p) (communicat### or interfac### or transfer####)	198	L5	Tue Feb 23 16:20:35 1999
JPO	l2 (p) (communicat### or interfac### or transfer####)	92	L4	Tue Feb 23 16:19:26 1999
JPO	l2 and (communicat### or interfac### or transfer####)	104	L3	Tue Feb 23 16:18:20 1999
JPO	process### (p) (programmable) (p) (bus### or line#)	231	L2	Tue Feb 23 16:15:06 1999
JPO	process### (p) (programmable(w) cell#) (p) (bus### or line#)	0	L1	Tue Feb 23 16:12:44 1999

Z39.50 Gateway Based on **CNIDR** Isite

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Search Results - *0 Hits.*

Term	Occurrence
L4 AND (DATA/BI (0W) FLOW/BI (0W) PROCESSOR#/BI)	0
PROCESS###/BI	423537
PROGRAMMABLE/BI	11565
BUS###/BI	22151
LINE#/BI	175790
COMMUNICAT###/BI	79739
INTERFAC###/BI	28702
TRANSFER####/BI	93819
L2 (0P) (COMMUNICAT###/BI OR INTERFAC###/BI OR TRANSFER####/BI)	198
DATA/BI	516631
FLOW/BI	152399
PROCESSOR#/BI	26063
DATA/BI (0W) FLOW/BI (0W) PROCESSOR#/BI	18

Database: US Patents / Japanese Patents / European Patents / USOCR Patents

Refine Search:

```
l4  and (data(w) flow(w) processor#)
```

Search History

DB Name	Query	Hit Count	Set Name	Time
EPO	l4 and (data(w) flow(w) processor#)	0	L7	Tue Feb 23 16:25:23 1999
JPO	l4 and (data(w) flow(w) processor#)	0	L6	Tue Feb 23 16:24:47 1999
EPO	l2 (p) (communicat### or interfac### or transfer####)	198	L5	Tue Feb 23 16:20:35 1999
JPO	l2 (p) (communicat### or interfac### or transfer####)	92	L4	Tue Feb 23 16:19:26 1999
JPO	l2 and (communicat### or interfac### or transfer####)	104	L3	Tue Feb 23 16:18:20 1999
JPO	process### (p) (programmable) (p) (bus### or line#)	231	L2	Tue Feb 23 16:15:06 1999
JPO	process### (p) (programmable(w) cell#) (p) (bus### or line#)	0	L1	Tue Feb 23 16:12:44 1999

Z39.50 Gateway Based on **CNIDR** Isite

```
ILE 'USPAT' ENTERED AT 13:16:49 ON 23 FEB 1999

  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
  *                                                               *
  *                  W E L C O M E   T O   T H E                  *
  *                                                               *
  *          U. S.   P A T E N T   T E X T   F I L E              *
  *                                                               *
  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

=> s process### (p) (programmable cell#) (p) (bus### or line#)

       1258537 PROCESS###
         65011 PROGRAMMABLE
        268633 CELL#
           224 PROGRAMMABLE CELL#
                 (PROGRAMMABLE(W)CELL#)
        139399 BUS###
       1468017 LINE#
L1           22 PROCESS### (P) (PROGRAMMABLE CELL#) (P) (BUS### OR LINE#)
```

d 1-2 cit hit

1. 5,480,823, Jan. 2, 1996, Method of making high density ROM, without using a code implant; Chen-Chung Hsu, 438/275, 297 [IMAGE AVAILABLE]

US PAT NO: 5,480,823 [IMAGE AVAILABLE] L4: 1 of 2

ABSTRACT:
A method of fabricating read only memory, (ROM), devices has been developed. This **process** is accomplished using self-alignment of buried N+ bit **lines**. Thick field oxides are used for isolation purposes. The **programmable cell** is obtained by growing a gate oxide in a region in which the thick field oxide has been removed. The non-**programmable cells** contain thick gate oxides. Polysilicon gate structures are **processed** to function as the word **lines**.

2. 5,113,498, May 12, 1992, Input/output section for an intelligent cell which provides sensing, bidirectional communications and control; Shabtai Evan, et al., 395/828; 364/221, 221.1, 228, 228.1, 231.8, 232.2, 232.8, 237.8, 238.3, 240, 240.8, 240.9, 241.9, 242.94, 242.96, 244, 244.3, 244.6, 244.9, 247, 247.2, 247.5, 247.6, 247.7, 247.8, 254, 254.5, 259, 259.1, 259.3, 259.5, 260, 260.3, 260.4, 260.81, 262, 262.3, 262.4, 262.9, 270, 271, 271.4, 271.5, 281.3, 284, 284.3, 284.4, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 5,113,498 [IMAGE AVAILABLE] L4: 2 of 2

ABSTRACT:
A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a **processor** and input/output section are coupled to the network. Each of the **programmable cells** receives when manufactured a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power **lines**, twisted, pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network. The preferred embodiment of the cell includes a multiprocessor and multiple I/O subsections where any of the **processors** can communicate with any of the I/O subsections. This permits the continual execution of a program without potential interruptions caused by interfacing with the I/O section. The I/O section includes programmable A-to-D and programmable D-to-A converters as well as other circuits for other modes of operation.

d l1 1,6,7,10,21 cit hit

1. 5,844,888, Dec. 1, 1998, Network and intelligent cell for providing sensing, bidirectional communications and control; Armas C. Markkula, Jr., et al., 370/255, 390, 400 [IMAGE AVAILABLE]

US PAT NO: 5,844,888 [IMAGE AVAILABLE] L1: 1 of 22

SUMMARY:

BSUM(10)

A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a **processor** and input/output section are coupled to the network. Each of the **programmable cells** receives when manufactured a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power **lines**, twisted pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network.

6. 5,475,687, Dec. 12, 1995, Network and intelligent cell for providing sensing, bidirectional communications and control; Armas C. Markkula, Jr., et al., 395/200.54; 370/419; 395/182.02 [IMAGE AVAILABLE]

US PAT NO: 5,475,687 [IMAGE AVAILABLE] L1: 6 of 22

SUMMARY:

BSUM(10)

A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a **processor** and input/output section are coupled to the network. Each of the **programmable cells** receives when manufactured a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power **lines**, twisted pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network.

7. 5,343,471, Aug. 30, 1994, Address filter for a transparent bridge interconnecting local area networks; Robert Cassagnol, 370/401 [IMAGE AVAILABLE]

US PAT NO: 5,343,471 [IMAGE AVAILABLE] L1: 7 of 22

DETDESC:

DETD(40)

Referring now to FIG. 7, an overall block diagram of the filter and its interface with respect to the RAM 15 is shown. The filter itself comprises a programmable logic device such as the Xilinx **programmable cell** for carrying out the foregoing functions. The filter 11 is connected by a data **bus** 61 with the RAM 15, as well as the host **processor** 14. Similarly, an address **bus** 62 is shared to permit either the filter or **processor** to access the RAM 15.

10. 5,113,498, May 12, 1992, Input/output section for an intelligent cell which provides sensing, bidirectional communication and control; Shabtai Evan, et al., 395/828; 364/221, 221.1, 228, 228.1, 231.8, 232.2, 232.8, 237.8, 238.3, 240, 240.8, 240.9, 241.9, 242.94, 242.96, 244, 244.3, 244.6, 244.9, 247, 247.2, 247.5, 247.6, 247.7, 247.8, 254, 254.5, 259, 259.1, 259.3, 259.5, 260, 260.3, 260.4, 260.81, 262, 262.3, 262.4, 262.9, 270, 271, 271.4, 271.5, 281.3, 284, 284.3, 284.4, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 5,113,498 [IMAGE AVAILABLE] L1: 10 of 22

ABSTRACT:
A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a **processor** and input/output section are coupled to the network. Each of the **programmable cells** receives when manufactured a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power **lines**, twisted, pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network. The preferred embodiment of the cell includes a multiprocessor and multiple I/O subsections where any of the **processors** can communicate with any of the I/O subsections. This permits the continual execution of a program without potential interruptions caused by interfacing with the I/O section. The I/O section includes programmable A-to-D and programmable D-to-A converters as well as other circuits for other modes of operation.

SUMMARY:

BSUM(10)

A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a **processor** and input/output section are coupled to the network. Each of the **programmable cells** receives when manufactured a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power **lines**, twisted pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network.

21. 4,782,340, Nov. 1, 1988, Electronic arrays having thin film line drivers; Wolodymyr Czubatyj, et al., 340/825.83, 825.81; 345/92, 205 [IMAGE AVAILABLE]

US PAT NO: 4,782,340 [IMAGE AVAILABLE] L1: 21 of 22

SUMMARY:

BSUM(24)

Those building thin film electronic arrays of various types have long desired to fully integrate the circuitry performing the addressing function, including the driving of address **lines** and any addressing circuitry such as address decoding, with the electronic array being serviced by such circuitry. Full integration, that is, the fabrication of the address decoding and **line** driving circuitry on the same substrate with the electronic matrix using thin film semiconductor **processing** techniques, is expected to lower the over-all manufacturing cost and reduce the size of such arrays, while at the same time improving their reliability. One important technical problem blocking such full integration and which has heretofore not been satisfactorily overcome is the relatively low power capability of most thin film devices, particularly their low current capability. In electronic arrays, particularly very large arrays having many locations or **programmable cells** connected to one conductor or address **line**, relatively high

amounts of current must be passed to and/or from such **lines** in a relatively short period of time, especially at the beginning or end of an access cycle for an individual address **line**. A typical 640 column by 400 row thin film liquid crystal display matrix used as a television, for example, and refreshed at 60 Hertz must update 24,000 rows per second, or one row every 40 microseconds. Commercially acceptable solid-state memories, such as random access memories (RAMs) or electrically erasable programmable read only memories (EEPROMs), require **line** access cycle times that are typically one to three orders of magnitude faster. As the number of cells connected to one **line** increases, the capacitance and current requirements of that **line** increase, exacerbating the foregoing current and speed problems.

```
s (wire# or conductor# or line#) (p) process### (p) cell#

        363565 WIRE#
        195413 CONDUCTOR#
       1500513 LINE#
       1291644 PROCESS###
        277475 CELL#
L10      18259 (WIRE# OR CONDUCTOR# OR LINE#) (P) PROCESS### (P) CELL#

=> s l10 (p) programm####

        171665 PROGRAMM####
L11       1094 L10 (P) PROGRAMM####

=> s l10 (p) (programm#### (3a) cell#)

        171665 PROGRAMM####
        277475 CELL#
L12        339 L10 (P) (PROGRAMM#### (3A) CELL#)
```